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TITLE OF INVENTION: A Single RIE Process for MIMCAP Top and Bottom Plates

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

A SINGLE RIE PROCESS FOR MIMCAP TOP AND BOTTOM PLATES

TECHNICAL FIELD

The present invention relates generally to the fabrication of semiconductor devices, and more particularly to metal-insulator-metal (MIM) capacitors.

BACKGROUND OF THE INVENTION

Semiconductors are widely used for integrated circuits for electronic applications, including radios, televisions and personal computing devices, as examples. Such integrated circuits typically use multiple transistors fabricated in single crystal silicon. It is common for there to be millions of semiconductor devices on a single semiconductor product. Many integrated circuits now include multiple levels of metallization for interconnections.

One type of semiconductor device is a MIM capacitor, which comprises a bottom capacitive plate formed in a metallization layer, a top capacitive plate in an overlying layer, the top and bottom plates being separated by a capacitor dielectric layer. MIM capacitors are used frequently in mixed signal devices and logic devices, for example.

A problem with manufacturing MIM capacitors is that the capacitor dielectric separating the two capacitive plates is very thin, e.g., 500 to 700 Angstroms thick. This can result in very high leakage currents due to conductive particles, e.g. from etching the plates, that may be present at the site of the capacitor dielectric. As a result, MIM capacitor designs typically comprise a top metal plate that is smaller in area than the bottom metal plate to prevent high leakage currents and shorts.

Because most MIM capacitors have this step-like construction from the bottom to top plates, a separate

lithography and etch step is required to form each of the top and bottom capacitor plates. This requires the use of two masks, two lithography steps, and two etch steps, one each for the bottom plate and the top plate.

What is needed in the art is a method of manufacturing MIM capacitors that has fewer etch steps, reduced complexity and a cost reduction compared to prior art MIM capacitor manufacturing methods.

SUMMARY OF THE INVENTION

These problems are generally solved or circumvented by the present invention, which achieves technical advantages as a method of simultaneously forming top and bottom plates of a MIM capacitor. A first resist is used to provide the pattern for the bottom metal plate, and a second resist is used to provide the pattern for the top metal plate of a MIM capacitor. The combined patterns of the first and second resist is simultaneously transferred to the underlying metallization layers in a single reactive ion etch (RIE) process.

Disclosed is a method of patterning metal layers of a semiconductor wafer, the method comprising depositing a first conductive layer over a substrate, depositing an insulating layer over the first conductive layer, depositing a second conductive layer over the insulating layer, depositing a first resist over the second conductive layer, depositing a second resist over the first resist, patterning the first resist with a first pattern, patterning the second resist with a second pattern, and simultaneously transferring the first pattern to the first conductive layer and the second pattern to the second conductive layer.

Also disclosed is a method of patterning metal layers of a semiconductor wafer, the wafer comprising a first conductive layer, an insulating layer disposed over

the first conductive layer and a second conductive layer disposed over the insulating layer. The method comprises depositing a first resist over the second conductive layer, patterning the first resist with a first pattern, depositing a second resist over the first resist, patterning the second resist with a second pattern, and simultaneously transferring the first pattern to the first conductive layer and transferring the second pattern to the second conductive layer.

Further disclosed is a method of forming capacitive plates of a MIM capacitor, comprising providing a wafer having a substrate, depositing a first conductive layer on the substrate, depositing a capacitor dielectric layer over the first conductive layer, depositing a second conductive layer over the capacitor dielectric layer, depositing a first resist over the second conductive layer, patterning the first resist with a first pattern, depositing a second resist over the first resist, patterning the second resist with a second pattern, simultaneously transferring the first pattern to the first conductive layer and transferring the second pattern to the second conductive layer.

Advantages of the invention include providing a method of transferring the pattern of top and bottom metal plates simultaneously, resulting in less manufacturing process complexity. The invention results in fewer defects, reduced throughput and lower manufacturing costs. With the use of the single RIE pattern transfer method in accordance with the present invention, one RIE step, one resist strip, and one cleaning step may be eliminated in the manufacturing process for a MIM capacitor. The invention also results in improved yields because there is less chance of misalignment of the top and bottom capacitive plates.

BRIEF DESCRIPTION OF THE DRAWINGS

The above features of the present invention will be more clearly understood from consideration of the following descriptions in connection with accompanying drawings in which:

Figures 1 through 7 illustrate cross-sectional views of a MIM capacitor in various stages of manufacturing in accordance with an embodiment of the present invention.

Corresponding numerals and symbols in the different figures refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments, and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A description of preferred embodiments of the present invention will be discussed, followed by some advantages. Four MIM capacitors are shown in each figure, although many MIM capacitors and other conductive lines may be present within each layer.

Referring to Figure 1, a workpiece 10 is provided, typically comprising silicon oxide over single-crystal silicon. The workpiece 10 may include other conductive layers or other semiconductor elements, e.g. transistors, diodes, etc. Compound semiconductors such as GaAs, InP, Si/Ge, SiC, as examples, may be used in place of silicon.

A first metallization layer 12 is deposited over the workpiece 10. First metallization layer 12 preferably comprises a conductive material such as Al, TiN, Ti, W, combinations thereof, or other conductive materials, as examples, deposited by physical vapor deposition (PVD) or chemical vapor deposition (CVD). Metallization layer 12 may comprise an M1 or M2 metallization layer, for example.

A dielectric layer 14 is deposited over the first metallization layer 12. Dielectric layer 14 preferably comprises an insulator such as a capacitor dielectric and may comprise saline oxide, tetraethoxysilane (TEOS), silicon dioxide, silicon nitride, silicon oxynitride, barium strontium titanate (BST) or other insulators, as examples.

A second metallization layer 16 is deposited over dielectric layer 14. Second metallization layer 16 preferably comprises Al, TiN, Ti, W, combinations thereof, or other conductive materials, as examples.

A first resist 18 is deposited over second metallization layer 16, as shown in Figure 2. First resist 18 is patterned by lithography, for example, with a mask, not shown. Preferably, first resist 18 comprises a negative resist; for example, first resist 18 preferably comprises CGR or other negative resists. The first resist 18 is exposed and developed. The first resist 18 pattern preferably comprises the pattern for the bottom capacitor plate for a MIM capacitor, to be described further herein.

A second resist 20 is deposited over exposed portions of second metallization layer 16 and the first resist 18, as shown in Figure 3a and 3b. Second resist 20 may be conformal as shown in Figure 3a, or alternatively, may conform to the pattern of the first resist 18, as shown in Figure 3b. Preferably, second resist 20 comprises a positive resist such as UV82, for example.

Second resist 20 is patterned by lithography with the pattern for the MIM capacitor top plates. Second resist 20 is patterned, for example, using a mask, not shown, and exposed portions of the second resist 20 are developed, stripped and cleaned, leaving the structure shown in Figure 4. The resulting structure comprises a

two-layer resist including first resist 18 and second resist 20. The second resist 20 is disposed over the first resist 18 and has a smaller pattern than the first resist 18.

The semiconductor wafer is exposed to a single reactive ion etch (RIE) process, as shown in Figure 5. A RIE chemistry 22, preferably comprising Cl_2, BCl_3, N_2, argon, or a combination thereof may be used, for example, when aluminum and TiN are used as conductive materials for the first metallization layer 12 and second metallization layer 16. Alternatively, an RIE gas 22 such as SF_6 may be used when W is used for the conductive material of the first and second metallization layers 12 and 16. Alternatively, other RIE gases 22 may be used for the single RIE etch of the present invention, such as HF and others, for example.

As the wafer is exposed to the RIE gas 22, a top portion of the second resist 20 is eroded away, shown generally at 26. Edge portions 24 of the first resist 18 not disposed beneath the second resist 20 are also eroded by the RIE gas 22. The RIE gas 22 simultaneously transfers the pattern from first resist 18 to second metallization layer 16 and dielectric layer 14, as shown in Figure 5.

Continued exposure of the wafer to RIE gas 22 results in continued erosion of the top portion 26 of second resist 20 and edge portions 24 of first resist 18, in addition to further transferring of the patterns of the first and second resists 18 and 20 to underlying first and second metallization layers 12/16 and insulating layer 14, as shown in Figure 6. At this stage of exposure to the RIE gas 22, the pattern from second resist 20 is essentially transferred to first resist 18, as shown. As the RIE gas 22 etches the wafer, the resulting structure is shown in Figure 7, with the

initial pattern of the second resist 20 being transferred to the second metallization layer 16 to form top plates 16, and the initial pattern of the first resist 18 being evident and transferred to the first metallization layer 12 and the dielectric layer 14.

After the MIM capacitors are formed, the wafer is then exposed to a chemical such as oxygen plasma until the first resist is completely stripped, followed by a wet clean to remove any residuals, as shown in Figure 7.

The present invention disclosed herein achieves technical advantages as a method of patterning top and bottom plates of a MIM capacitor that requires a single RIE step, which reduces the manufacturing complexity and results in the cost reduction for a semiconductor wafer. Critical dimensions (CD) of the patterning of the MIM capacitors are relaxed because the size of these capacitors are relatively large, a few micrometers for example. Hence, the pattern transfer is not required to be precise as in the prior art. The invention results in fewer defects and increased throughput. With the use of the single RIE pattern transfer in accordance with the present invention, one RIE step, one resist strip, and one cleaning step may be eliminated. The invention also results in a yield improvement.

The invention has been described herein with first resist 18 comprising a negative resist and second resist 20 comprising a positive resist. Alternatively, first resist 18 may comprise a positive resist, and second resist 20 may comprise a negative resist.

While the present invention has been described in detail herein with reference to a MIM capacitor, the present invention may also be used in semiconductor manufacturing applications where two or more metallization layers are required to be patterned on a single semiconductor device. In particular, an

application where a lower metallization layer will be patterned with a larger pattern than an overlying smaller metallization pattern, the present invention is particularly advantageous. More broadly, the invention can be used in any semiconductor devices where there are two patterns on top of each other that require two successive lithography and RIE processes.

While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications in combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. In addition, the order of process steps may be rearranged by one of ordinary skill in the art, yet still be within the scope of the present invention. It is therefore intended that the appended claims encompass any such modifications or embodiments. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.